Abstract ~~ABSTR~~

Dual interleaved DC to DC switching circuits realizable in an integrated circuit form, capable of monitoring individual inductor current using only one current sense resistor and providing automatic duty cycle adjustment to keep the inductor currents in the interleaved DC to DC switching circuits balanced. The preferred embodiment includes a gain error amplifier, an integral error amplifier, and a differentiator error amplifier and circuits for controlling the nominal duty cycle, with the gain error amplifier, integral error amplifier and differentiator error amplifier being adjustable independently by external components. The circuit further includes a high speed load regulation circuit that momentarily overrides the control circuitry to take over control of the interleaved converters during sudden load changes, such control also being programmable. The circuit further includes a load variation circuit to target the output voltage of the circuit to an optimal value with load to better keep the output voltage within a targeted range in the event of major step changes in the load. The disclosed embodiment is for two interleaved buck converters, though the principles of the invention are applicable to interleaved step up converters and the interleaving of more than two converters.